

Programming the AD9833/AD9834

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INTRODUCTION

This application note describes how to program a sinusoidal waveform on the output of the AD9833/AD9834 parts. The sequence involves entering reset mode, entering data into the Freq0 register, and exiting reset mode.

PROGRAMMING THE AD9833/AD9834

When the AD9833/AD9834 is powered up, the part should be reset. This resets appropriate internal registers to 0 to provide an analog output of midscale. To avoid spurious DAC

outputs while the AD9833 is being initialized, the RESET bit should be set to 1 until the part is ready to begin generating an output. The RESET bit does not reset the phase, frequency, or control register. These registers will contain invalid data, and, therefore, should be set to a known value by the user. The RESET bit should then be set to 0 to begin generating an output. The data appears on the DAC output eight MCLK cycles after RESET is set to 0.

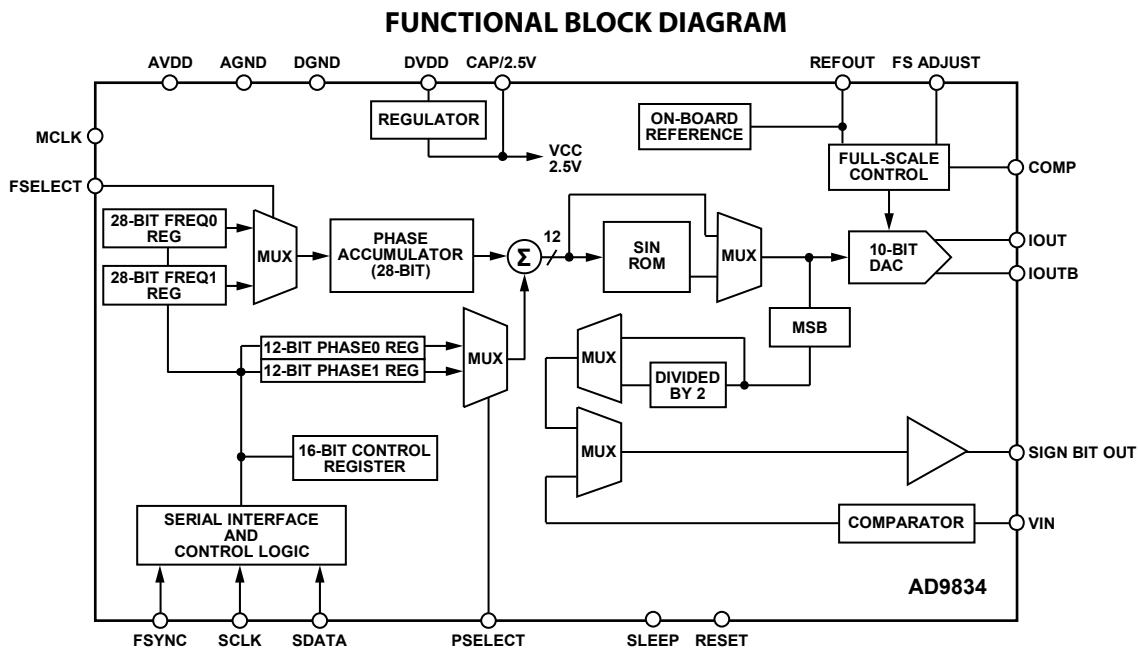


Figure 1. AD9834 Functional Block Diagram

08955-001

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MORE ON PROGRAMMING THE AD9833/AD9834

A simple example is the best method to explain how to program the AD9833/AD9834. Refer to the AD9833 or the AD9834 data sheet for more details.

Basic Example

The aim is to generate a 400 Hz output frequency using the AD9833 with a 25 MHz MCLK.

The dial-up code for this is defined by the equation

$$FreqReg = \frac{f_{OUT} \times 2^{28}}{f_{MCLK}}$$

Thus, for this example, $Freq\ 0 = 400\ Hz$.

$$FreqReg = \frac{400\ Hz \times 2^{28}}{25\ MHz}$$

$$= 4295\ decimal = 0x10C7 = 0001\ 0000\ 1100\ 0111$$

The required initialization sequence is shown in Table 1.

Table 1.

Hexadecimal	Binary
0x2100	0010 0001 0000 0000
0x50C7	0101 0000 1100 0111
0x4000	0100 0000 0000 0000
0xC000	1100 0000 0000 0000
0x2000	0010 0000 0000 0000

Command Sequence Explained

0x2100—Control Register

- DB13 is set to 1. This allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains 14 LSBs. The second write contains 14 MSBs.
- RESET bit DB8 is set to 1. This resets internal registers to 0, which corresponds to an analog output of midscale.

0x50C7—Frequency Register 0 LSB

- DB15 and DB14 are set to 0 and 1, respectively, which is the Frequency Register 0 address.
- The remaining 14 bits are the 14 LSBs of data:
0x10C7 = 01 0000 1100 0111

0x4000—Frequency Register 0 MSB

- DB15 and DB14 are set to 0 and 1, respectively, which is the Frequency Register 0 address.
- The remaining 14 bits are the 14 MSBs of data and are all 0s in this case.

0xC000—Phase Register 0

- DB15, DB14, and DB13 are set to 110, with DB12 set to don't care (X), respectively, which is the address for Phase Register 0.
- The remaining 12 bits are the data bits and are all 0s in this case.

0x2000—Exit Reset

- A signal appears at the output of the DAC seven MCLK cycles after RESET is set to 0.

NOTES